Q.P. Code : 541502

(3 Hours) [Total Marks : 80

N.B. : (1) Question **No.1** is **compulsory**.
(2) Solve **any three** questions out of remaining five questions.
(3) Assume suitable **data** if **necessary**.

1. Attempt **any four** out of **five questions**.
(a) Explain Von Neumann architecture in detail. 5
(b) Explain various pipeline hazards with example. 5
(c) Differentiate between Computer Organization & Architecture. 5
(d) Explain Flynn's Classification. 5
(e) What are the differences between RISC and CISC processors. 5

2. (a) Convert $(127.125)_{10}$ in IEEE-754 single and double precision floating point representation. 10
(b) Explain micro instruction sequencing and execution. 10

3. (a) Calculate the hit and miss using various page replacement policies LRU, OPTIMAL, FIFO for following sequence (page frame size = 3) 4, 7, 3, 0, 1, 7, 3, 8, 5, 4, 5, 3, 4, 7. State which one is best for above example? 10
(b) Explain the importance of multiple bus hierarchies with the help of suitable diagram. 10

4. (a) Describe Hardwired Control Unit and specify its advantages. 10
(b) Describe the characteristics of Memory. 10

5. (a) Explain DMA based data transfer technique for I/O devices. 10
(b) Multiply (-7) with (4) by using Booth's algorithm of Multiplication. 10

6. Write short notes on (**any four**) : 20
(a) Types of ROM
(b) Cache Coherency
(c) Scanner
(d) Interrupt driven I/O
(e) Nano Programming